K. L. E. Society's

K. L. E. Institute of Technology, Hubballi

Dept. of Electronics and Communication Engg.

List of events conducted under PHOENIX association for the year 2020-21

Sl.no	Event Name	Date	Target	PO Mapping
1	Talk on Career Guidance by Mr. Shreeraj B. Humbarwadi, H. R., 3M, Bengaluru	27/09/2020	3rd sem	PO- 1,9, 10
2	Guest lecture on "Network Analysis"	29/9/2020 to 04/10/2020	3rd sem	PO – 8, 12
3	Placement orientation program by Prof.Tejas K.R	08/10/2020	7th sem	PO- 12
4	Webinar on "Physical design of VLSI chips"	07/12/2020	7th sem	PO – 1, 2,9
5	A workshop on "Introduction to Basic Components and Multisim 8"	14/12/2020	3rd sem	PO – 5, 6, 12
6	Workshop on "Machine learning and deep learning" from Mathworks and Corl Technologies, Bengaluru.	18/01/2021	7th sem	PO – 1,8,9
7	"Workshop on LabVIEW" by Prashant Hanasi	30/09/2021	5th sem	PO-5, 6, 12

Mr. Rakesh H.M

Pheonix Co-ordinator

Dr. Manu T M

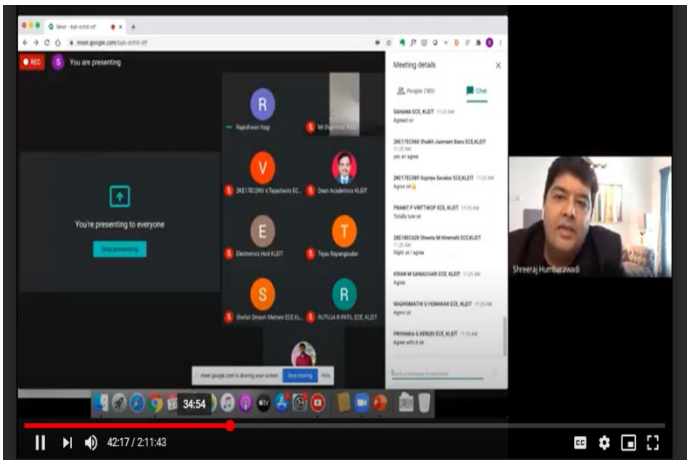
HOD

Report: Talk on Career Guidance

A talk on "Career Guidance" was conducted under PHOENIX on 27/09/2020 for 3rd semester students. The resource person for the talk was Shreeraj B. Humbarwadi, H. R., 3M, Bengaluru.

The talk was to provide a comprehensive, developmental program designed to assist individuals in making and implementing informed educational and occupational choices. The guidance given to individuals helps them acquire the knowledge, information, skills, and experience necessary to identify career options and narrow them down to make one career decision. This career decision then results in their social, financial, and emotional well-being throughout. The following are the important suggestions given for the students to build their careers.

1. Seek internship opportunities.
2. Consider taking part in a work-study program.
3. Grow your skills and knowledge.
4. Get an early start.
5. Keep your skills up-to-date.
6. Stay focused.
7. Find a balance with your personal life.
8. Pursue your passion.
9. Strive for excellence and stay motivated.
10. Use your school's career services.



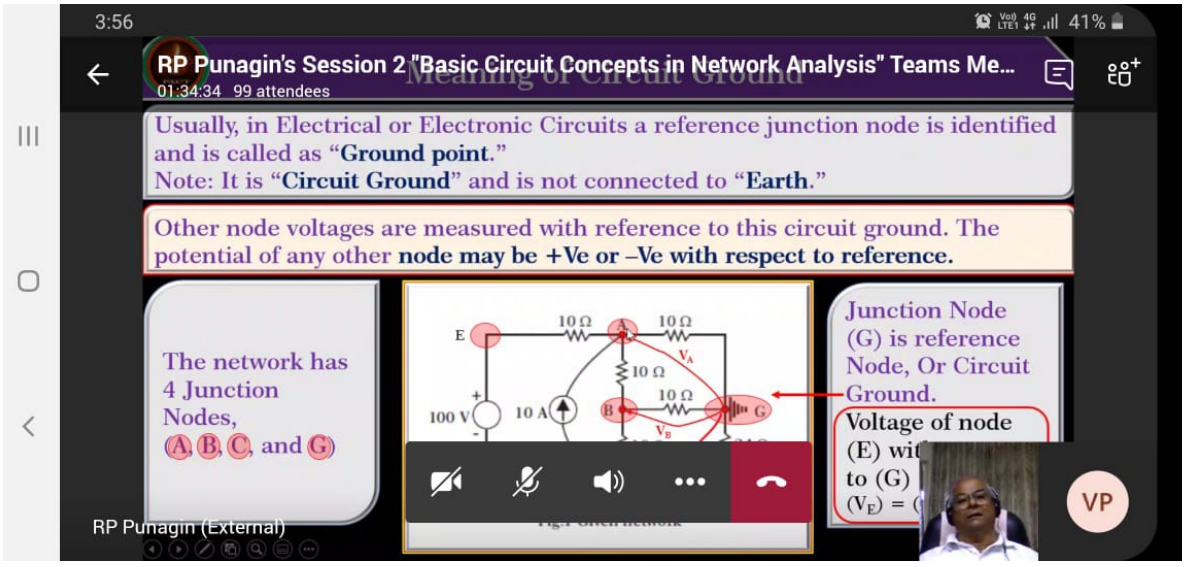
Mr. Shreeraj B. Humbarwadi explaining about career guidance

Report: Guest lecture on Network Analysis

A guest lecture on **"Network analysis"** was conducted from 29/9/2020 to 04/10/2020 for III semester students. The resource person was Prof. R.P Punagin. It was focused on the transient analysis of dc and ac circuits and initial conditions.

The speaker ignited the thoughts on network analysis with many videos on-

1. Basic concepts with circuits on network theory
2. Network terminology
3. Voltage and current sources
4. Transient analysis of dc and ac circuits
5. Initial conditions



Prof. R.P Punagin explaining about basic circuit concepts in network analysis

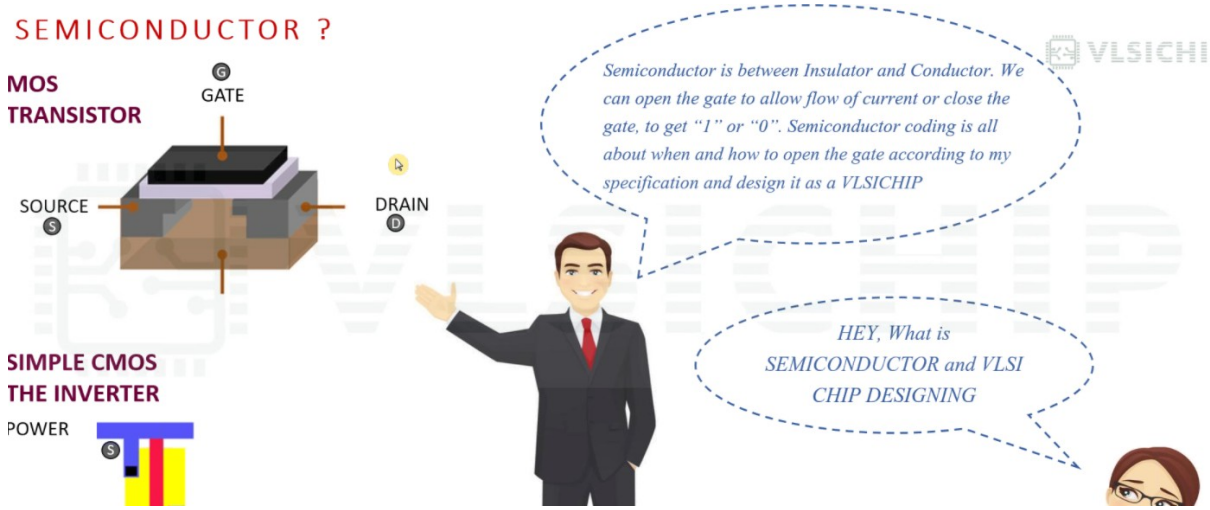
Report: Placement orientation program

A session on **"Placement orientation"** program was conducted on 8/10/2020 in the department of ECE. The talk was given by Mr. Tejas K.R., Asst. Professor of ECE dept, KLET, Hubballi. It was arranged for 7th-semester students. The session focused on the skills that are required by the students regarding the placement process and informing students about current trends in industries. It also focused on preparation that is required before facing the interviews.

Webinar on "Physical design of VLSI chips"

Webinar on "Physical design of VLSI Chips" was conducted for 7th semester students on 7/12/2020. The resource persons were George Jacob and Kumar. K VLSI Chip technologies, Bangalore. The following topics were discussed.

Semiconductor growth: The semiconductor industry has been growing exponentially every year and offers a plethora of opportunities. But this year, the semiconductor industry is set to face a host of new challenges that will make it difficult for semiconductor manufacturers to grow at the same rate they have gotten used to over the past couple of years Challenges pertaining to inventory management and the rising pressure to improve device architectures, reduce costs, and develop STEM skills in the workforce will inhibit the growth of companies to a certain degree.



1. **Physical design :** Physical design directly impacts circuit performance, area, reliability, power, and manufacturing yield

- **Performance**: long routes have significantly longer signal delays.
- **Area**: placing connected modules far apart results in larger and slower chips.
- **Reliability:** A large number of vias can significantly reduce the reliability of the circuit.
- **Power:** transistors with smaller gate lengths achieve greater switching speeds at the cost of higher leakage current and manufacturing variability; larger transistors and longer wires result in greater dynamic power dissipation.
- **Yield**: wires routed too close together may decrease yield due to electrical shorts occurring during manufacturing, but spreading gates too far apart may also undermine yield due to longer wires and a higher probability of opens.
- **Partitioning:** breaks up a circuit into smaller sub-circuits or module which can each be designed or analyzed individually.
- **Floorplanning:** determines the shapes and arrangement of sub-circuits or modules, as well as the locations of external ports and IP or macro-blocks
- **Power and ground routing (power planning)**: often intrinsic to floorplanning, distributes power (VDD) and ground (GND) nets throughout the chip.
- **Placement:** finds the spatial locations of all cells within each block.
- **Clock network synthesis:** determines the buffering, gating (e.g., for power management) and routing of the clock signal to meet prescribed skew and delay requirements
- **Global routing:** allocates routing resources that are used for connections; example resources include routing tracks in the channel and in the switch box

- **Detailed routing**: assigns routes to specific metal layers and routing tracks within the global routing resources.
- **Timing closure:** optimizes circuit performance by specialized placement or routing techniques

2. **Physical verification:**
   After physical design is completed, the layout must be fully verified to ensure correct electrical and logical functionality. Some problems found during physical verification can be tolerated if their impact on chip yield is negligible. Therefore, at this stage, layout changes are usually performed manually by experienced design engineers.
3. **Design rule checking (DRC):** verifies that the layout meets all technology-imposed constraints. DRC also verifies layer density for chemical-mechanical polishing (CMP).
4. **Layout vs. schematic (LVS):** checking verifies the functionality of the design. From the layout, a netlist is derived and compared with the original netlist produced from logic synthesis or circuit design.
5. **Parasitic extraction:** derives electrical parameters of the layout elements from their geometric representations; with the netlist, these are used to verify the electrical characteristics of the circuit.
6. **Antenna rule checking:** seeks to prevent antenna effects, which may damage transistor gates during manufacturing plasma-etch steps through the accumulation of excess charge on metal wires that are not connected to PN junction node
7. **Electrical rule checking (ERC):** verifies the correctness of power and ground connections, and that signal transition times (slew), capacitive loads and fan-outs are appropriately bounded

Report: Talk on "Introduction to Basic Electronic Components"

A talk on **"Introduction to Basic Electronic Components"** was conducted under PHOENIX on 14/12/2020 for 3rd semester students. The resource person for the talk was Mr. Datta, Proprietor, Unique solutions, Hubballi.

The talk was to provide an overview of both theoretical and practical aspects of electronic components. The theory session was related to the components such as resistors, capacitors, BJT, MOSFET, diodes, and some concepts on PCB designing. The practical session included the software simulation of simple circuits, working of series and parallel circuits, to check LED operations, and demonstration of working of some circuit examples. It also included the designing of circuits using active and passive elements in the system software using Multisim-8 software.

Report: Workshop on "Machine learning and deep learning"

A one-day workshop on **"Machine learning and deep learning"** was conducted under PHOENIX on 18/01/2021 for 5th semester students from Mathworks and Corl Technologies, Bengaluru. The following topics were discussed.

1. Overview of Machine Learning.
2. Introduction to Neural Networks and Fundamental concepts of Deep Learning.
3. Domain generation algorithms (DGA) and uniform resource locator (URL) Data Analysis applying Machine Learning.
4. Applications of Machine Learning and Deep Learning.