# Dr.Rakesh H.M #6 Shakti colony,2nd stage

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**Career Objective**

A responsible and challenging position that will allow me to explore my abilities and skills and sense of dedication towards my duties with a aim of seeing the progress of the organisation and to adapt to the changing organisation needs with changing global scenario.

**Academic Qualifications**

|  |  |  |  |
| --- | --- | --- | --- |
| Course | **University / Institute** | **Year of Passing** | **Percentage** |
| Ph.D | VTU | 2024 | **-** |
| **M.Tech** in **VLSI Design And Testing** | BVBCET,Hubli | 2012 | 8.91(CGPA) |
| B.E. in Electronics & Communication | RYMEC, Bellary | 2009 | 70% |
| Class XII | Karnataka State Board | 2005 | 75.16% |
| **Class X** | Karnataka State Board | 2003 | 85.60% |

**Technical Skills**

* Designing using Cadence
* Designing using NGspice
* Assembly Language: Microprocessor 8085, 8086, Microcontroller 8051
* Programming Language: C
* Operating Systems: Windows 9X/2000/XP, Linux

**Subjects of Interest**

* Low Power VLSI Circuits
* Testing and Verification of VLSI Circuits
* Logic Design
* Analog and Mixed Mode VLSI Circuits

**Tools Known**

Cadence, NGspice, Matlab, Kiel C51, Xilinx.

**Working Experience Details:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name of the Institute** | **Designation** | **Date of Joining** | **Date of Reliving** | **Total Working Experience** |
| K.L.E Institute of Technology | Associate Professor | August 2013 | Till Date | 11 years |

**Subject Handled:**

* Basic Electronics.
* Analog Electronic Circuits.
* VLSI Design.
* Verilog HDL.
* Microprocessors.
* CAD for VLSI.

**Department level responsibilities:**

* Student association “PHOENIX” Coordinator.
* Technical fest “Advitiya” Coordinator.
* Mentorship coordinator for the academic year 2018-19, 2019-20.
* Website Coordinator.
* NBA Criterion 2, Criterion 8 Coordinator.

**FDP’s/Workshops attended:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Sl.No** | **Course title** | **Institute** | **Period/Duration** |
| 1 | FDP on “LABVIEW” | KLEIT, Hubballi | 25th-26th March 2021/2 days |
| 2 | FDP on “CADENCE” | KLEIT, Hubballi | 11th -13th May 2019/3 days |
| 3 | FDP on “VLSI Physical Design & Verification” | KLEIT, Hubballi | 25th -27th July 2019/3 days |
| 4 | FDP on “Image Processing” | KLEIT, Hubballi | 24th -28th July 2018/5 days |
| 5 | FDP on “Signal processing” | KLETECH, Hubballi | 15th -20th July 2017/1 week |
| 6 | FDP on “Enhancing Analytical Skills in Basic Electronics” | KLE TECH University, Hubballi | 3th -4th  November 2017/2 days |
| 7 | FDP on “CMOS Mixed Signal and Radio Frequency VLSI Design” | KLEIT, Hubballi | 26th -30th December 2017/5 days |
| 8 | Workshop on Outcome Based  Education | KLEIT, Hubballi | 24th- 25th January 2014/2 days |
| 9 | ISTE workshop on signals and systems | IIT, Kharagpur | 14th -20th March 2013/7 days |
| 10 | FDP on signals and systems | BVBCET, Hubballi | 16th -28th December 2013/14 days |

**Coursera/Udemy/NPTEL Courses completed:**

* **Programming for everybody(Getting started with python).**
* **Introduction to IoT and embedded systems.**
* **AI for everyone.**
* **FPGA Computing systems.**

**Technical papers published:**

* Dr. G.S. Sunitha, Rakesh H.M, “Design and Implementation of adder architectures and analysis of performance metrics”, International Journal of Electronics and Communication Engineering and Technology (IJECET), Volume 8, Issue 5, pp.1–6, Sep-Oct2017.
* Rakesh H.M, Dr. G.S. Sunitha, “Design and Implementation of Vedic and Booth multiplier on spartan 3”, International Journal of VLSI Design, Microelectronics and Embedded System, Volume 2,Isuue 2 ,pp.34-40, Dec 2017.
* Rakesh H.M, Dr. G.S. Sunitha, “Comparative analysis of 16 x 16 bit Vedic and Booth multipliers”, World Journal of Technology, Research and Engineering(WJTER), Volume 3, Issue 1,pp.305-313, Jan 2018.
* Rakesh H.M, Dr. G.S. Sunitha, “Performance Comparison of Conventional multiplier with Vedic Multiplier using ISE simulator”, International Journal of Engineering and Manufacturing Science, ISSN 2249-3115 Volume 8, Number 1 ,pp. 95-103,2018.
* Rakesh H.M, Dr. G.S. Sunitha, “ A Survey on Architectures of MAC units for DSP Applications, “ European Journal of Advances in Engineering and Technology”, Volume 6,Issue 4,pp.36-39,2019.
* Rakesh H.M, Dr. G.S. Sunitha, “Design and implementation of Novel 32-Bit MAC unit for DSP Applications, “IEEE International Conference for Emerging Technology”,June 5-7, 2020.*DOI:10.1109/INCET49848.2020.9154177*

**Major Project in M.Tech**

**Title:** Design and implementation of 8X8 SRAM.

**Tools:** Cadence

**Description:**Design of 64 bit SRAM in cadence to perform both read and write operation and test its read and write access time.

**Minor Project in M.Tech**

**Title:** Design of PCI Bus

**Tools:** Xilinx 12.1, Cadence

**Description:**To design the peripheral **component interconnect** bus which is used to connect the slave devices to the main system bus. And test its functionality.

**Mini Projects in M.Tech**

**Project #1**

**Title:** Design of Current Mirror Circuit.

**Tools:** Cadence Design Tool

**Description:**Current mirror are simply an extension of the current sink/source. The current mirror uses the principle that if that gate-source potentials of two identical MOS transistors are equal, the channel currents should be equal.

**Project #2**

**Title:**Design and power analysis of static latches for low power VLSI

**Tools:** NGSpice for simulation

**Description:** Design of Static Latches for low power consumption using NGspice and verifying the results by comparing them with the values present in IEEE papers.

**Project #3**

# Title:ADC TLV1578 Characterization

**Description:** Generation of analog inputs to the ADC TLV1578 using sample and hold circuit and IC LF398.

**Final-Year Project in Bachelor of Engineering**

**Title**: College radio using amplitude modulation technique

**Description**: The objective is to make a college or any private institution to own a radio station for the purpose of communication within its private area at a very cheaper cost for both educational and entertainment purposes.

**Personal Details**

**Date of Birth :** January 30, 1987

**Language Proficiency :** English, Hindi & Kannada.

**Hobbies :** PlayingCricket, Badminton, Listening to music.

Rakesh H.M